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(71) Applicant: **FUJITSU LIMITED**
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)
(71) Applicant: **FUJITSU VLSI LIMITED**
1844-2, Kozoji-cho 2-chome
Kasugai-shi Aichi 487 (JP)

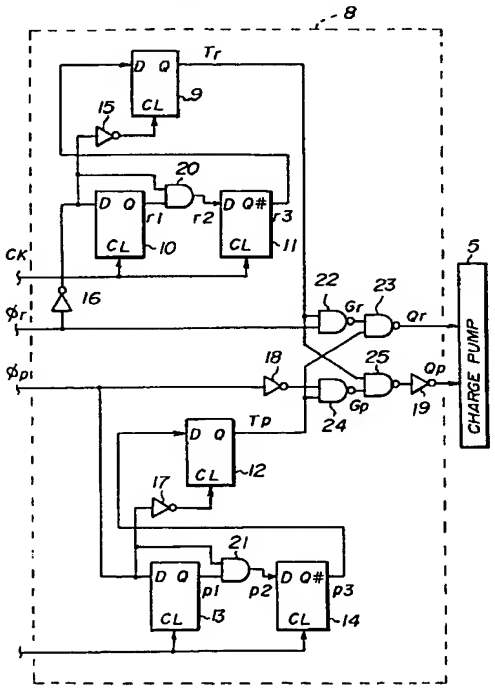
(72) Inventor: **Saito, Shinji**
c/o Fujitsu VLSI Ltd., 1844-2, Kozoji-cho 2-chome
Kasugai-shi, Aichi 487 (JP)
Inventor: **Kobayashi, Akira**
c/o Fujitsu VLSI Ltd., 1844-2, Kozoji-cho 2-chome
Kasugai-shi, Aichi 487 (JP)

(74) Representative: **Joly, Jean-Jacques et al**
CABINET BEAU DE LOMENIE 55, rue d'Amsterdam
F-75008 Paris (FR)

(54) PLL synthesizer circuit.

(57) The circuit uses a lowpass filter (6) including capacitors (61, 62) for restricting an output voltage of the lowpass filter, a charge pump circuit (5) for controlling the output voltage of the lowpass filter by charging or discharging the capacitors of the lowpass filter, a voltage controlled oscillator (VCO) (7) controlled by the output voltage of the lowpass filter, a frequency divider (3) operating on the VCO output to supply a comparison signal, a phase comparator (4) signal to output phase error information which indicates a phase lead and a phase lag of the comparison signal with respect to the reference signal. According to the invention, a charge pump control circuit (8) forms control information based on the phase error information when switching a frequency of the output signal of the VCO from a first frequency to a second frequency and supplies the control information to the charge pump circuit. The charge pump circuit (5) charges or discharges the capacitors of the lowpass filter (6) independently of the reference signal based on the control information until the VCO output reaches the second frequency, so as to raise or lower the output voltage of the lowpass filter depending on the charging or discharging. The output signal of the voltage controlled oscillator is used as an output signal of th PLL synthesizer circuit.

FIG.7



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BACKGROUND OF THE INVENTION

The present invention generally relates to phase locked loop (PLL) synthesizer circuits, and more particularly to a PLL synthesizer circuit in which an output signal frequency of a voltage controlled oscillator can be switched at a high speed.

FIG.1 shows an example of a conventional PLL synthesizer circuit. The PLL synthesizer circuit includes a crystal oscillator 1, a reference frequency divider 2, a comparison frequency divider 3, a phase comparator 4, a charge pump circuit 5, a lowpass filter 6, and a voltage controlled oscillator (VCO) 7 which are connected as shown. The reference frequency divider 2 frequency-divides an output signal of the crystal oscillator 1 and outputs a reference signal Sr. The comparison frequency divider 3 frequency-divides an output signal SVCO of the VCO 7 and outputs a comparison signal Sp. The phase comparator 4 compares the phases of the reference signal Sr and the comparison signal Sp, and outputs signals for adjusting an output voltage VLPF of the lowpass filter 6 via the charge pump circuit 5 so that the phase error becomes zero. The charge pump circuit 5 outputs a signal SCP. The output signal SVCO of the VCO 7 is locked to a target frequency, and this output signal SVCO of the VCO 7 is output as an output signal of the PLL synthesizer circuit.

The phase comparator 4 is of the so-called phase discrimination type, and discriminates the phase lag and phase lead of the comparison signal Sp with respect to the reference signal Sr. The phase comparator 4 outputs a signal ør which indicates the phase lag of the comparison signal Sp with respect to the reference signal Sr and a signal øp which indicates the phase lead of the comparison signal Sp with respect to the reference signal Sr and a signal øp. The signals ør and øp are output independently from the phase comparator 4.

For example, the charge pump circuit 5 and the lowpass filter 6 have a construction shown in FIG.2. When the signals ør and øp both have a low level in FIG.2, a PNP transistor 51 turns ON and an NPN transistor 52 turns OFF, thereby making a charging operation with respect to capacitors 61 and 62. On the other hand, when the signals ør and øp both have a high level in FIG.2, the PNP transistor 51 turns OFF and the NPN transistor 52 turns ON, thereby making a discharging operation with respect to the capacitors 61 and 62. When the signal ør has the high level and the signal øp has the low level, the transistors 51 and 52 both turn OFF and the capacitors 61 and 62 enter a floating state. In this case, the charged voltages are held by the capacitors 61 and 62, and the output voltage VLPF of the lowpass filter 6 stabilizes.

FIGS.3 and 4 are timing charts for explaining the operation of the charge pump circuit 5 of the conventional PLL synthesizer circuit shown in FIG.1. FIG.3 shows the timing chart for explaining the operation of the charge pump circuit 5 when the frequency dividing ratio of the comparison frequency divider 3 is increased from the state where the output signal SVCO of the VCO 7 is locked to a frequency f1 and the output signal SVCO locks to a frequency f2 which is greater than the frequency f1, where fr denotes the frequency of the reference signal Sr and Fp denotes the frequency of the comparison signal Sp. FIG.4 shows the timing chart for explaining the operation of the charge pump circuit 5 when the frequency dividing ratio of the comparison frequency divider 3 is decreased from the state where the output signal SVCO of the VCO 7 is locked to the frequency f2 and the output signal SVCO locks to the frequency f1.

As may be seen from FIGS.3 and 4, the falling edge of the phase comparison signal ør is synchronized to the rising edge of the reference signal Sr regardless of whether the PLL synthesizer circuit is in the locked state or the unlocked state. In addition, the rising edge of the phase comparison signal øp is synchronized to the rising edge of the comparison signal Sp regardless of whether the PLL synthesizer circuit is in the locked state or the unlocked state.

However, when the frequency dividing ratio of the comparison frequency divider 3 is increased from the state where the output signal SVCO of the VCO 7 is locked to the frequency f1 and state changes to the unlocked state where fr>fp, the low-level period of the phase comparison signal ør is enlarged by a width which is slightly greater than the phase delay of the comparison signal Sp with respect to the reference signal Sr as shown in FIG.3 in a state where the falling edge of the phase comparison signal ør remains synchronized to the rising edge of the reference signal Sr. In this case, the rising edge of the phase comparison signal øp remains synchronized to the rising edge of the comparison signal Sp, and no change occurs as for the high-level period of the phase comparison signal øp.

As a result, the charge pump circuit 5 intermittently turns ON the PNP transistor 51 in synchronism with the rising edge of the reference signal ør, and intermittently supplies a charge voltage to the lowpass filter 6. Hence, the output voltage VLPF of the lowpass filter 6 rises, and the frequency of the output signal SVCO of the VCO 7 increases to the frequency f2.

When the frequency of the output signal SVCO of the VCO 7 rises to the frequency f2, the frequency fr of the reference signal Sr and the frequency fp of the comparison signal Sp become equal (that is, fr=fp), and the phase comparison signal ør returns to a state which indicates that there is no phase error between the reference signal Sr and the comparison signal Sp. Consequently, the capacitances 61 and 62 of the lowpass filter 6 assume the floating state, and the charged voltage in the capacitors 61 and 62 are held.

The utput voltage VLPF of th l wpass filter 6 stabilizes t th voltage at which th frequ ncy of th output signal SVCO of th VCO 7 becomes the frequ ncy f2, and the frequency f the output signal SVCO f th VCO 7 is locked to the frequency f2.

On the other hand, when the frequency dividing ratio of the comparison frequency divider 3 is decreased from the state where the output signal SVCO of the VCO 7 is locked to the frequency f2 and state changes to the unlocked state where fr<fp, the high-level period of the phase comparison signal øp is enlarged by a width which is slightly greater than the phase lead of the comparison signal Sp with respect to the reference signal Sr as shown in FIG.4 in a state where the falling edge of the phase comparison signal øp remains synchronized to the rising edge of the reference signal Sr. In this case, the falling edge of the phase comparison signal ør remains synchronized to the rising edge of the comparison signal Sp, and no change occurs as for the low-level period of the phase comparison signal ør.

As a result, the charge pump circuit 5 intermittently turns ON the NPN transistor 52 in synchronism with the rising edge of the comparison signal Sp, and intermittently discharges the capacitors 61 and 62 of the lowpass filter 6. Hence, the output voltage VLPF of the lowpass filter 6 falls, and the frequency of the output signal SVCO of the VCO 7 decreases to the frequency f1.

When the frequency of the output signal SVCO of the VCO 7 falls to the frequency f1, the frequency fr of the reference signal Sr and the frequency fp of the comparison signal Sp become equal (that is, fr=fp), and the phase comparison signal øp returns to a state which indicates that there is no phase error between the reference signal Sr and the comparison signal Sp. Consequently, the capacitances 61 and 62 of the lowpass filter 6 assume the floating state, and the charged voltage in the capacitors 61 and 62 are held. The output voltage VLPF of the lowpass filter 6 stabilizes to the voltage at which the frequency of the output signal SVCO of the VCO 7 becomes the frequency f1, and the frequency of the output signal SVCO of the VCO 7 is locked to the frequency f1.

When charging the capacitors 61 and 62 which form the lowpass filter 6 of the conventional PLL synthesizer circuit, the charging operation is intermittently carried out in synchronism with the reference signal Sr. In addition, the discharging operation is carried out intermittently in synchronism with the comparison signal Sp. For this reason, there is a problem in that the frequency of the output signal SVCO of the VCO 7 cannot be switched at a high frequency.

Presently, communication syst ms such as mobil tel phon sets are all analog systems. However, when such c mmunication systems are changed to digital systems, it becomes desirabl to tun to a desired frequency at a high sp d particularly in the case of a digital mobile teleph ne set. In th r words, th r is a demand to realiz a PLL synthsizer circuit in which th lock-up tim is extremely short.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful PLL synthesizer circuit in which the problem described above is eliminated and the above described demand is satisfied.

Another and more specific object of the present invention is to provide a PLL synthesizer circuit comprising a lowpass filter including capacitors for restricting an output voltage of the lowpass filter, a charge pump circuit, coupled to the lowpass filter, for controlling the output voltage of the lowpass filter by charging or discharging the capacitors of the lowpass filter, a voltage controlled oscillator, coupled to the lowpass filter, for outputting an output signal having a frequency which is controlled by the output voltage of the lowpass filter, a frequency divider, coupled to the voltage controlled oscillator, for frequency-dividing the output signal of the voltage controlled oscillator and for outputting a comparison signal, the frequency divider having a variable frequency dividing ratio, a phase comparator, coupled to the frequency divider, for comparing a phase of a reference signal having a predetermined frequency and a phase of the comparison signal output from the frequency divider, the phase comparator outputting phase error information which indicates a phase lead and a phase lag of the comparison signal with respect to the reference signal, and a charge pump control circuit, coupled between the phase comparator and the charge pump circuit, for forming control information based on the phase error information when switching a frequency of the output signal of the voltage controlled oscillator from a first frequency to a second frequency, and for supplying the control information to the charge pump circuit, where the charge pump circuit charges or discharges the capacitors of the lowpass filter independently of the reference signal based on the control information until the output signal of the voltage controlled oscillator reaches the second frequency, so as to raise or lower the output voltage of the lowpass filter depending on the charging or discharging, and the output signal of the voltage controlled oscillator is used as an output signal of the PLL synthesizer circuit. According to the PLL synthesizer circuit of the present invention, the output voltage of the lowpass filter can be raised and lowered at a high speed, thereby making it possibl t switch the output signal fr qu ncy of the voltag controll d scillator at a high speed.

Other objects and furth r f atures of th pres nt inv nti n will be apparent from the f llowing detailed

description wh n read in conjuncti n with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a system block diagram showing an example of a conventional PLL synthesizer circuit according to the present invention;

FIG.2 is a circuit diagram showing a charge pump circuit and a lowpass filter of the conventional PLL synthesizer circuit shown in FIG.1;

FIGS.3 and 4 are timing charts for explaining an operation of the conventional PLL synthesizer circuit shown in FIG.1;

FIG.5 is a system block diagram showing a first embodiment of a PLL synthesizer circuit according to the present invention;

FIG.6 is a system block diagram showing a second embodiment of the PLL synthesizer circuit according to the present invention;

FIG.7 is a circuit diagram showing a charge pump control circuit and a charge pump circuit shown in FIG.6;

FIGS.8 and 9 are timing charts for explaining an operation of the second embodiment;

FIG.10 is a timing chart for explaining the effects of the second embodiment;

FIG.11 is a system block diagram showing a third embodiment of the PLL synthesizer circuit according to the present invention; and

FIG.12 is a circuit diagram showing a charge pump circuit which may be used in the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First, a description will be given of a first embodiment of the PLL synthesizer circuit according to the present invention, by referring to FIG.5. In FIG.5, those parts which are the same as those corresponding parts in FIG.1 are designated by the same reference numerals.

The PLL synthesizer circuit shown in FIG.5 includes a comparison frequency divider 3, a phase comparator 4, a charge pump control circuit 8, a charge pump circuit 5, a lowpass filter 6, and a voltage controlled oscillator (VCO) 7 which are connected as shown. The comparison frequency divider 3 has a variable frequency dividing ratio and frequency-divides an output signal SVCO of the VCO 7 and outputs a comparison signal Sp. The phase comparator 4 is of the phase discrimination type and compares the phases of a ref rence signal Sr and th compari- s n signal Sp, and outputs phas c mparison signals ør and øp. The phase comparison signals ør and øp respectiv ly indicat the phase lead and phase lag of th comparison signal Sp with respect to th reference signal Sr. The charg pump circuit 5 charges or discharg s capacitors of the l wpass filter 6 so as to control an output voltage VLPF of th lowpass filter 6. Th frequency of th utput signal SVCO f the VCO 7 is controlled by the output voltage VLPF of the lowpass filter 6.

The charge pump control circuit 8 varies the frequency dividing ratio of the comparison frequency divider 3 and forms the phase comparison signals ør and øp into signals Qr and Qp for controlling the operation of the charge pump circuit 5 in response to an external clock signal CK when switching the frequency of the output signal SVCO of the VCO 7. In other words, the operation of the charge pump circuit 5 is controlled so that the output voltage VLPF of the lowpass filter 6 is raised or lowered by charging or discharging the capacitors of the lowpass filter 6 virtually without interruption until the frequency of the output signal SVCO of the VCO 7 reaches a target frequency.

The charging or discharging of the capacitors of the lowpass filter 6 for restricting the output voltage VLPF of the lowpass filter 6 is carried out virtually without interruption, that is, in an essentially continuous manner. For this reason, compared to the conventional PLL synthesizer circuit in which the charging or discharging is carried out intermittently, the output voltage VLPF of the lowpass filter 6 can be raised and lowered at a high speed in the PLL synthesizer circuit according to the present invention. Therefore, the frequency of the output signal SVCO of the VCO 7 can be switched at a high speed.

Next, a description will be given of a second embodiment of the PLL synthesizer circuit according to the present invention, by referring to FIG.6. In FIG.6, those parts which are the same as those corresponding parts in FIGS.1 and 5 are designated by the same reference numerals, and a description thereof will be omitted.

This embodiment of the PLL synthesizer circuit shown in FIG.6 differs from the conventional PLL synthesizer circuit shown in FIG.1 in that the charge pump control circuit 8 is provided between the phase comparator 4 and the charge pump circuit 5. This charge pump control circuit 8 controls the operation of the charge pump circuit 5 in response to the clock signal CK from the reference frequency divider 2. Otherwise, this embodiment of the PLL synthesizer circuit is basically the same as the conventional PLL synthesizer circuit.

For example, the charge pump control circuit 8 includes D flip-flops 9 through 14, inverters 15 through 19, AND circuits 20 and 21, and NAND circuits 22 through 25 which are connected as shown in FIG.7. In FIG.7, Q# d n tes an inv rted utput of th D flip-flops 11 and 14.

FIGS.8 and 9 are timing charts for explaining th peration of the second embodim nt. In FIGS.8 and

9, r1 denotes an output signal of the D flip-flop 10, r2 denotes an output signal of the AND circuit 20, r3 denotes an output signal of the D flip-flop 11, Tr denotes an output signal of the D flip-flop 9, Gr denotes an output signal of the NAND circuit 22, Qr denotes an output signal of the NAND circuit 23, p1 denotes an output signal of the D flip-flop 13, p2 denotes an output signal of the AND circuit 21, p3 denotes an output signal of the D flip-flop, Tp denotes an output signal of the D flip-flop 12, Gp denotes an output signal of the NAND circuit 24, and Qp denotes an output signal of the inverter 19.

FIG.8 shows the timings of the signals for explaining the operation when the frequency dividing ratio of the comparison frequency divider 3 is increased from the state where the output signal SVCO of the VCO 7 is locked to the frequency f1 and the output signal SVCO locks to the frequency f2 which is greater than the frequency f1.

On the other hand, FIG.9 shows the timings of the signals for explaining the operation when the frequency dividing ratio of the comparison frequency divider 3 is decreased from the state where the output signal SVCO of the VCO 7 is locked to the frequency f2 and the output signal SVCO locks to the frequency f1.

As may be seen from FIG.8, when the frequency dividing ratio of the comparison frequency divider 3 is increased from the state where the output signal SVCO of the VCO 7 is locked to the frequency f1 and state changes to the unlocked state where fr>fp, the charge pump circuit 5 supplies a charge voltage to the lowpass filter 6 during a time in which the reference signal Sr has a high level from a time when the unlocked state begins. Thereafter, the frequency of the output signal SVCO of the VCO 7 rises to the target frequency f2 from the time when the reference signal Sr next rises, and the capacitors 61 and 62 of the lowpass filter 6 are charged substantially without interruption until the phase of the comparison signal Sp and the phase of the reference signal Sr match. As a result, the output voltage VLPF of the lowpass filter 6 rises and the frequency of the output signal SVCO of the VCO 7 rises to the frequency f2.

When the frequency of the output signal SVCO of the VCO 7 rises to the frequency f2, the frequency fr of the reference signal Sr and the frequency fp of the comparison signal Sp become equal (that is, fr=fp). Hence, the phase comparison signal ør returns to the state which indicates that there is no phase error between the reference signal Sr and the comparison signal Sp, and the capacitors 61 and 62 of the lowpass filter assume the floating state. Consequently, the charged voltages in the capacitors 61 and 62 are held, and the utput voltag VLPF f th lowpass filter 6 stabiliz s to th voltag at which the frequ ncy f the output signal SVCO of the VCO 7 becomes the frequency f2, and the frequency f th utput signal SVCO of the VCO 7 locks to the frequency f2.

On th ther hand, as may be seen from FIG.9, wh n th frequ ncy dividing ratio of th comparison frequency divider 3 is d creased from th state where the output signal SVCO of the VCO 7 is locked to the frequency f2 and state changes to the unlocked state where fr<fp, the charge pump circuit 5 discharges the capacitors 61 and 62 of the lowpass filter 6 during a time in which the comparison signal Sp has a high level from a time when the unlocked state begins. Thereafter, the frequency of the output signal SVCO of the VCO 7 falls to the target frequency f1 from the time when the comparison signal Sp next rises, and the capacitors 61 and 62 of the lowpass filter 6 are discharged substantially without interruption until the phase of the comparison signal Sp and the phase of the reference signal Sr match. As a result, the output voltage VLPF of the lowpass filter 6 falls and the frequency of the output signal SVCO of the VCO 7 falls to the frequency f1.

When the frequency of the output signal SVCO of the VCO 7 falls to the frequency f1, the frequency fr of the reference signal Sr and the frequency fp of the comparison signal Sp become equal (that is, fr=fp). Hence, the phase comparison signal øp returns to the state which indicates that there is no phase error between the reference signal Sr and the comparison signal Sp, and the capacitors 61 and 62 of the lowpass filter assume the floating state. Consequently, the charged voltages in the capacitors 61 and 62 are held, and the output voltage VLPF of the lowpass filter 6 stabilizes to the voltage at which the frequency of the output signal SVCO of the VCO 7 becomes the frequency f1, and the frequency of the output signal SVCO of the VCO 7 locks to the frequency f1.

Therefore, according to this embodiment, the capacitors 61 and 61 (shown in FIG.2) of the lowpass filter 6 are charted or discharged substantially without interruption by providing the charge pump control circuit 8. For this reason, the output voltage VLPF of the lowpass filter 6 can be raised and lowered at a high speed compared to the conventional PLL synthesizer circuit in which the charging or discharging is carried out intermittently.

FIG.10 is a timing chart for explaining the change in the output signal SVCO of the VCO 7 when switching of the frequency of the output signal SVCO of the VCO 7 from the frequency f1 to the frequency f2. The change indicated by a dotted line in FIG.10 is obtained in the second embodiment of the PLL synthesizer circuit, while the change indicated by a solid line in FIG.10 is obtained in the conventional PLL synthesizer circuit. As may be seen from FIG.10, the output voltage VLPF of the l wpass filter 6 can be changed at a high sp d in th second mbodiment when compared to the conv ntional PLL synth sizer circuit.

Next, a descripti n will be given of a third embodiment of the PLL synthesizer circuit according to the

pres nt invention, by referring to FIG.11. In FIG.11, thos parts which are th same as thos corresponding parts in FIG.6 are designated by th same refer- nce num rals, and a description thereof will be omitted.

In this embodiment, a phase comparator 40 outputs a phase error signal ø which indicates the phase error between the reference signal Sr and the comparison signal Sp. For example, this phase error signal ø may be a tri-level signal. A charge pump control circuit 80 forms the signals Qr and Qp based on the phase error signal ø, and supplies these signals Qr and Qp to the charge pump circuit 5. Of course, the charge pump control circuit 80 may form a tri-level control signal based on a tri-level phase error signal ø and control the charge pump circuit 5 by the tri-level control signal.

The charge pump circuit 5 which is used in the first through third embodiments is not limited to that shown in FIG.2, and various other charge pump circuits may be used. FIG.12 shows a charge pump circuit 5 which may also be used in the first through third embodiments. In FIG.12, P-channel MOSFET 510 and an N-channel MOSFET 520 are used in place of the PNP transistor 51 and the NPN transistor 52 shown in FIG.2, and the resistors shown in FIG.2 are omitted.

Claims

1. A phase locked loop synthesizer circuit comprising a lowpass filter (6) including capacitors (61, 62) for restricting an output voltage of the lowpass filter; a charge pump circuit (5), coupled to the lowpass filter, for controlling the output voltage of the lowpass filter by charging or discharging the capacitors of the lowpass filter; a voltage controlled oscillator (7), coupled to the lowpass filter, for outputting an output signal having a frequency which is controlled by the output voltage of the lowpass filter; a frequency divider (3), coupled to the voltage controlled oscillator, for frequency-dividing the output signal of the voltage controlled oscillator and for outputting a comparison signal, said frequency divider having a variable frequency dividing ratio; and a phase comparator (4), coupled to the frequency divider, for comparing a phase of a reference signal having a predetermined frequency and a phase of the comparison signal output from the frequency divider, said phase comparator outputting phase error information which indicates a phase lead and a phas lag of the comparison signal with resp ct to the ref rence signal, characteriz d in that there is provided: a charge pump control circuit (8), coupl d betwe n the phase comparator (4) and th charg pump circuit (5), for f rming control information based on the phase error information wh n switching a frequency of th output signal of th voltag controlled oscillator (7) from a first frequency to a second frequency, and for supplying the control information to th charge pump circuit, that said charge pump circuit (5) charges or discharges the capacitors of the lowpass filter (6) independently of the reference signal based on the control information until the output signal of the voltage controlled oscillator (7) reaches the second frequency, so as to raise or lower the output voltage of the lowpass filter depending on the charging or discharging, and that the output signal of the voltage controlled oscillator (7) is used as an output signal of the phase locked loop synthesizer circuit.

2. The phase locked loop synthesizer circuit as claimed in claim 1, characterized in that said charge pump control circuit (8) forms the control information based on the phase error information in response to an external clock signal.

3. The phase locked loop synthesizer circuit as claimed in claim 1, characterized in that there are further provided a crystal oscillator (1) for outputting a predetermined signal and a reference frequency divider (2) for frequency-dividing the predetermined signal to output the reference signal together with a clock signal, and said charge pump control circuit (8) forms the control information based on the phase error information in response to the clock signal.

4. The phase locked loop synthesizer circuit as claimed in any of claims 1 to 3, characterized in that said charge pump circuit (5) charges or discharges the capacitors (61, 62) of the lowpass filter (6) substantially without interruption based on the control information.

5. The phase locked loop synthesizer circuit as claimed in any of claims 1 to 4, characterized in that said phase comparator (4) outputs the phase error information which is made up of a first signal which indicates the phase lead of the comparison signal with respect to the reference signal and a second signal which indicates the phase lag of the comparison signal with respect to the reference signal.

6. The phase locked loop synthesizer circuit as claimed in claim 5, characterized in that said charg pump control circuit (8) outputs th control inf rmation which is mad up of a third signal which corresponds to th first signal and a fourth signal which corresponds to the second signal.

7. The phase locked loop synthesizer circuit as claimed in claim 5, characterized in that said charge pump circuit (5) includes first and second transistors (51, 52; 510, 520) of mutually pposite transistor types coupled in series between a power source and ground, and said first and second transistors are respectively controlled based on the first and second signals.

8. The phase locked loop synthesizer circuit as claimed in claim 7, characterized in that said first and second transistors (51, 52) respectively are PNP and NPN transistors.

9. The phase locked loop synthesizer circuit as claimed in claim 7, characterized in that said first and second transistors (510, 520) respectively are p-channel and N-channel MOSFETS.

10. The phase locked loop synthesizer circuit as claimed in claim 7, characterized in that said first and second transistors (51, 52; 510, 520) of the charge pump circuit (5) are coupled to each other at a node, and said lowpass filter (6) receives the output signal of the charge pump circuit via the node.

FIG. 1 PRIOR ART

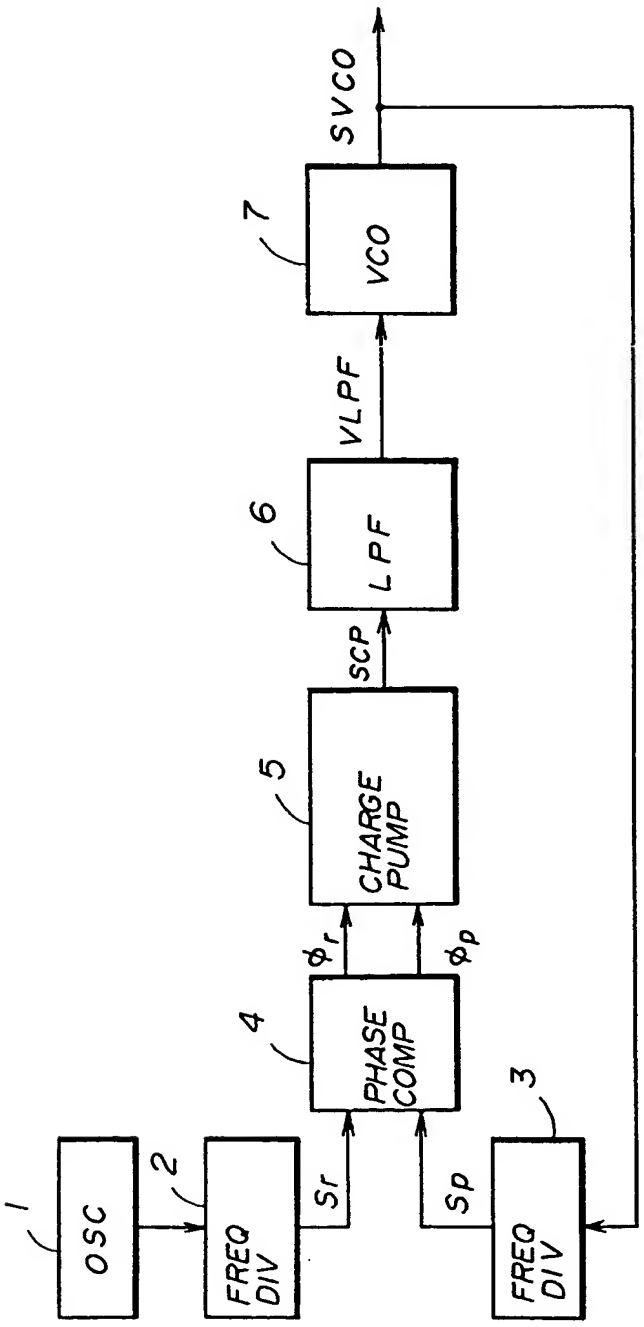


FIG.2 PRIOR ART

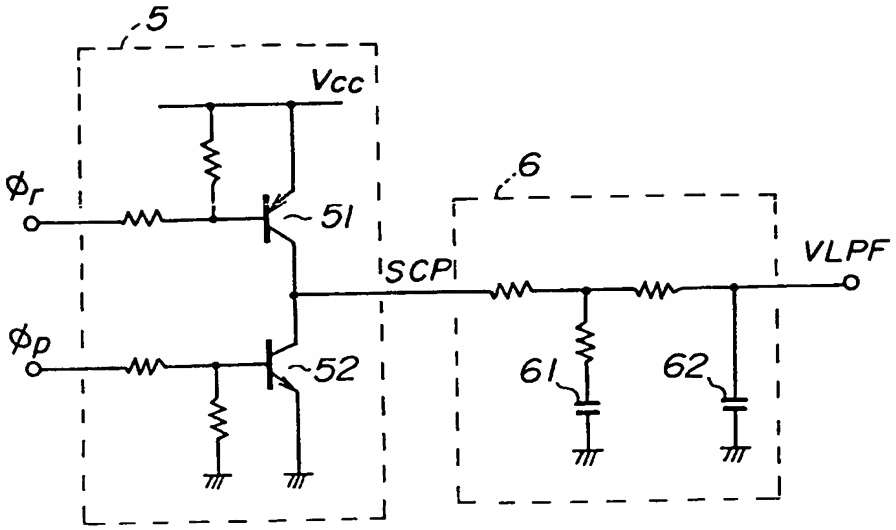


FIG.12

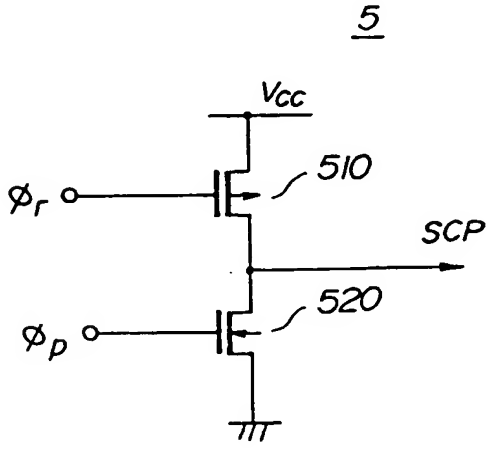


FIG.3 PRIOR ART

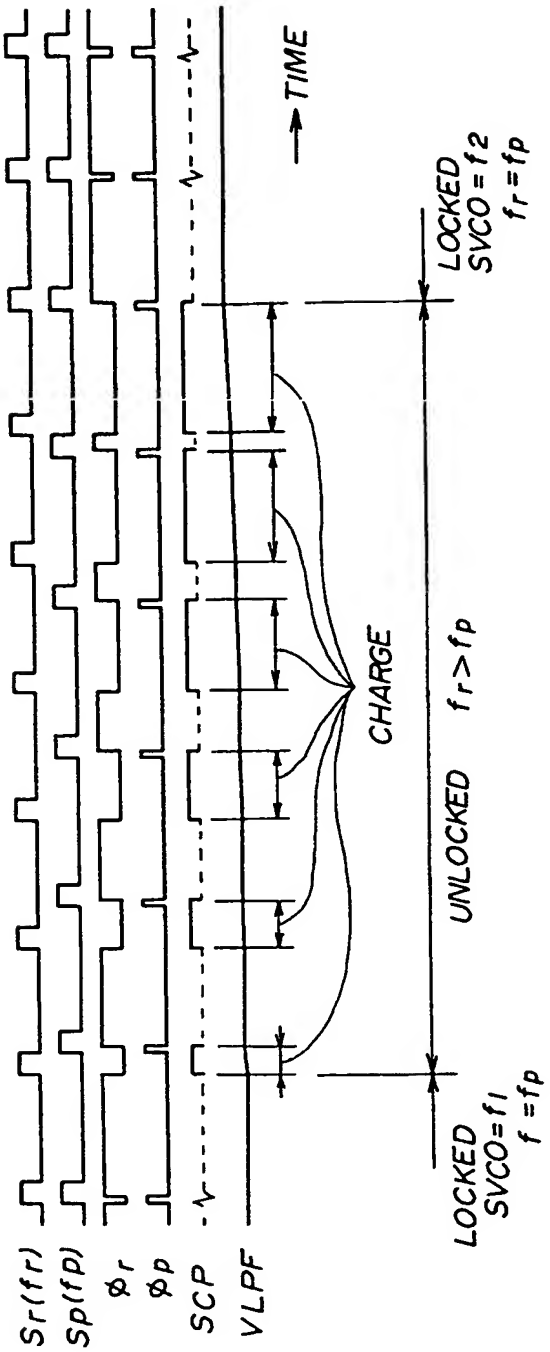


FIG.4 PRIOR ART

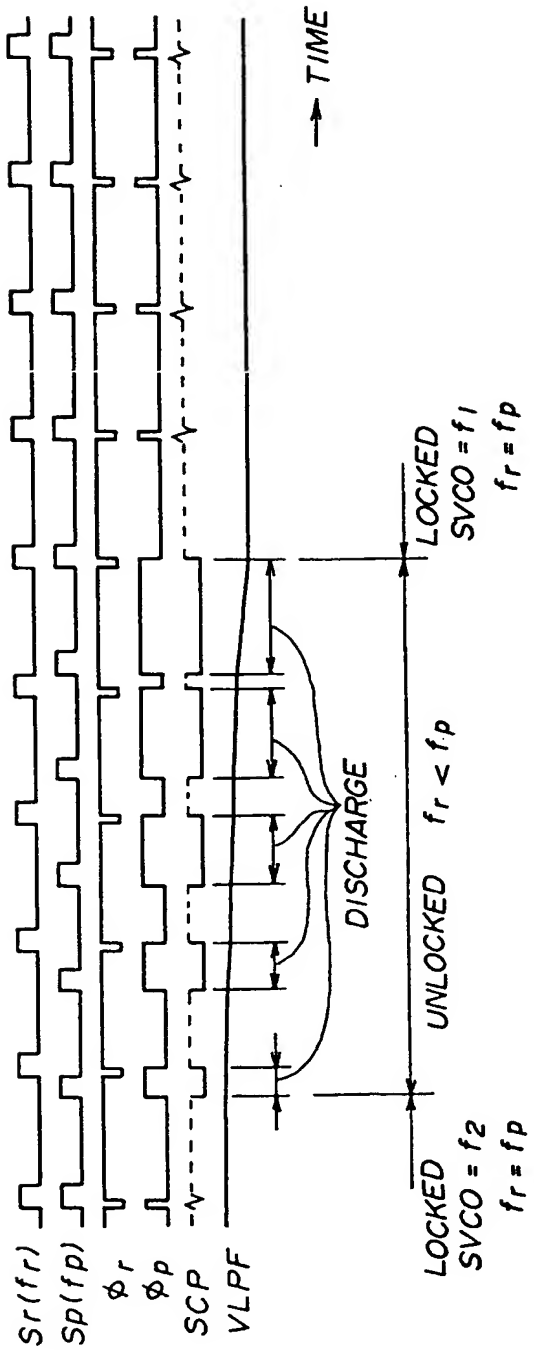


FIG.5

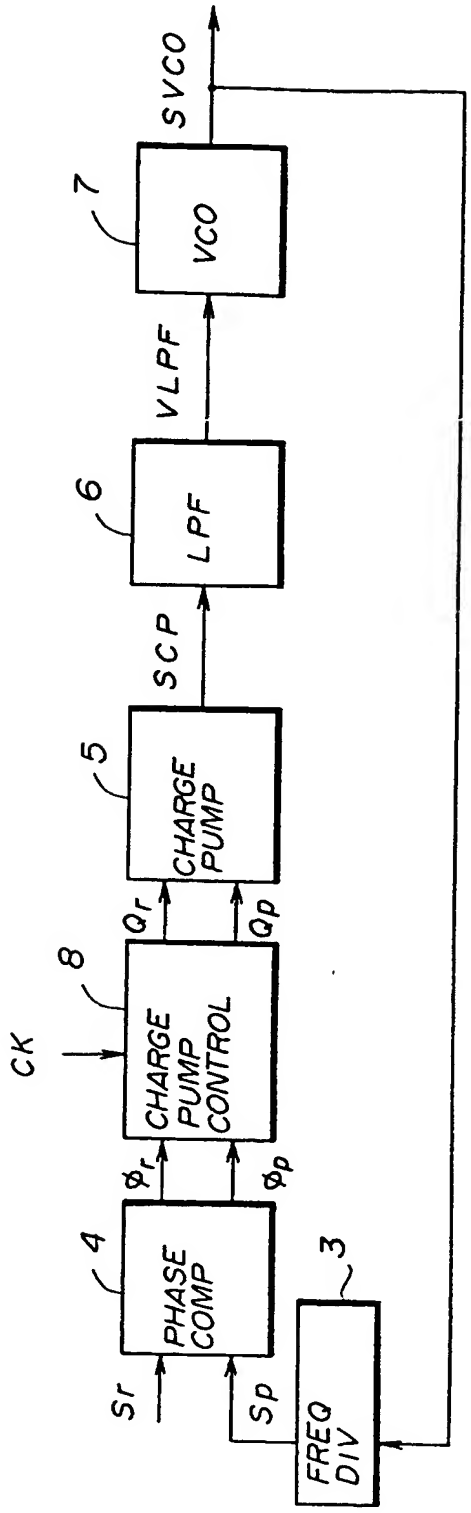
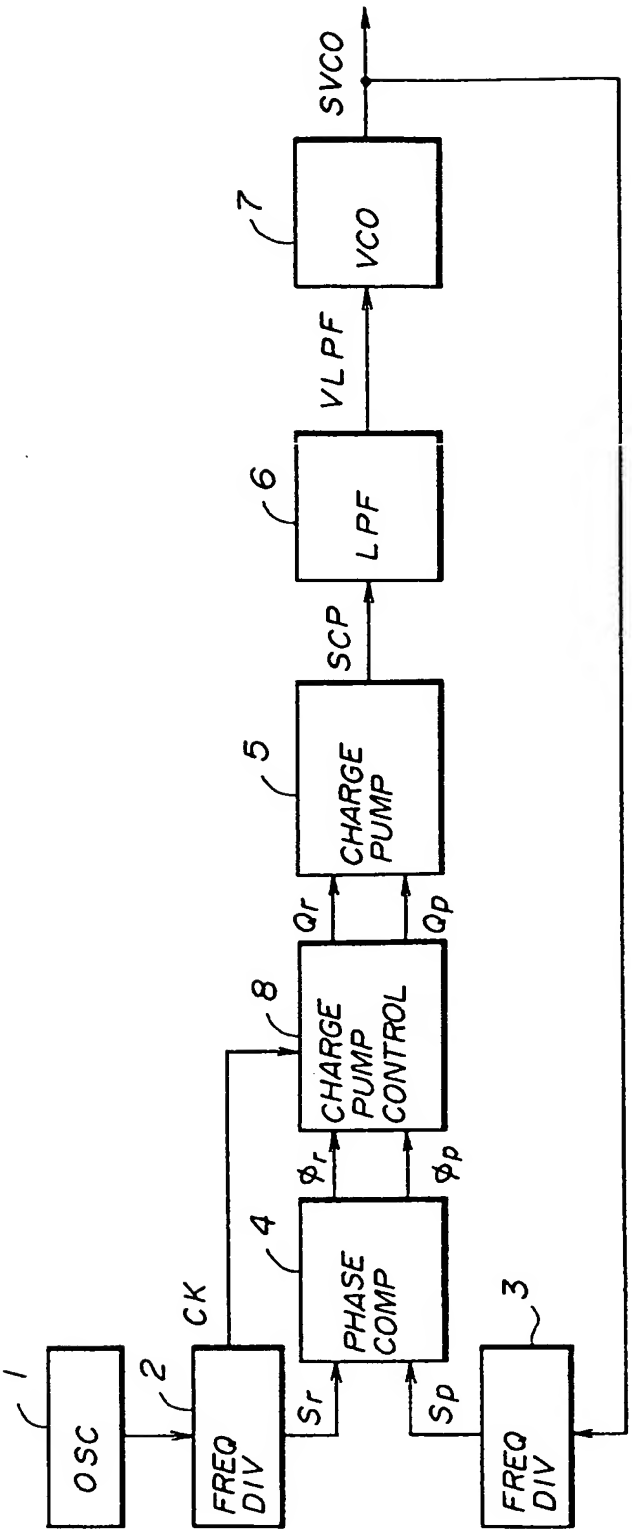

SVCO
7
VCO
VLPF
6
LPF
SCP
5
CHARGE PUMP
Qr
Qp
8
CHARGE PUMP CONTROL
CK
φr
φp
4
PHASE COMP
3
FREQ DIV
Sr
Sp

FIG.6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CHARGE PUMP
5
LPF
6
VCO
7
CHARGE PUMP CONTROL
8
Sr
Sp
Qr
Qp
SCP
VLPF
SVCO
φr
φp

FIG.7

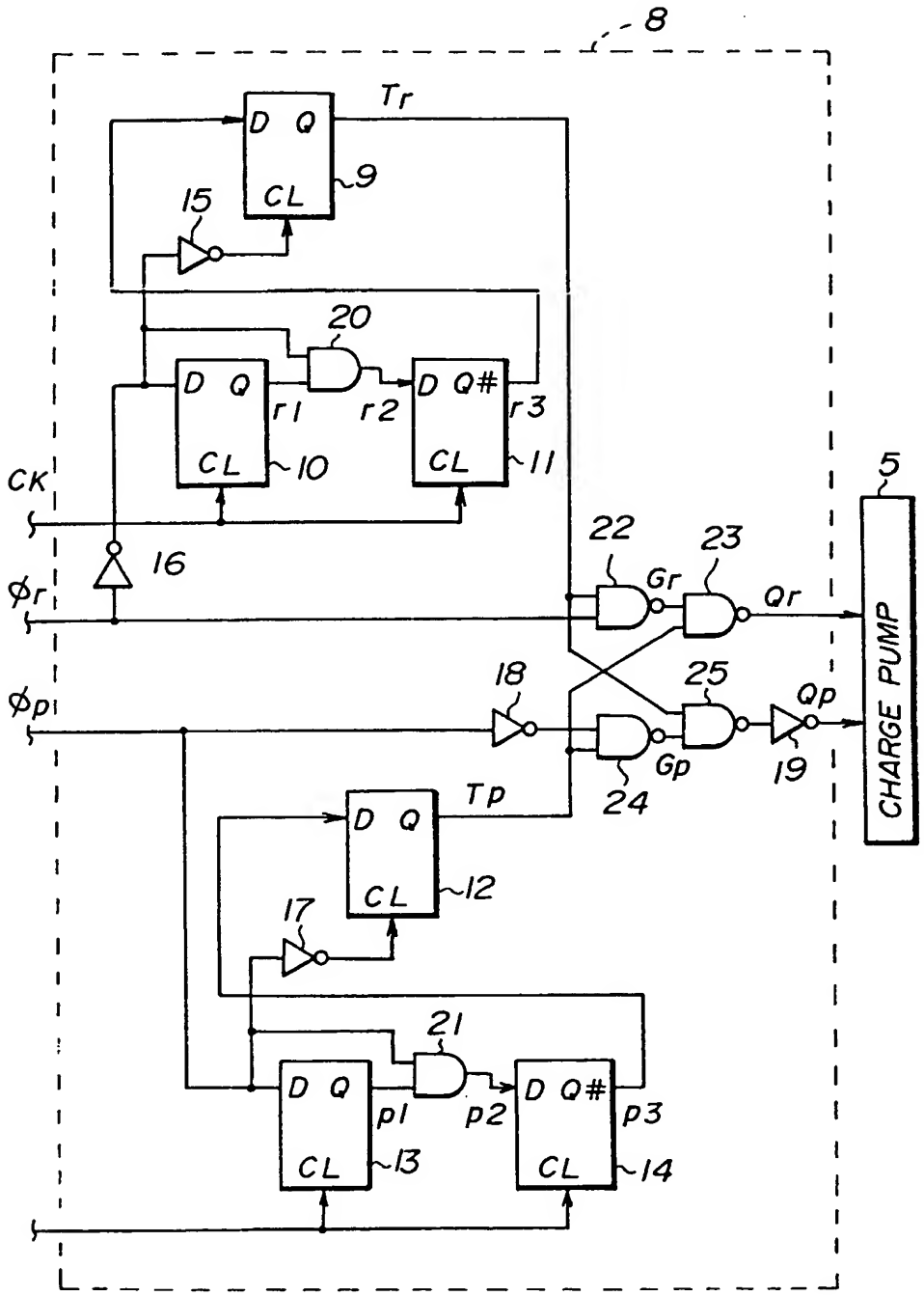

8
Tr
D Q
CL
9
15
20
D Q
r1
r2
D Q#
r3
CL
10
CL
11
CK
16
22
23
Gr
Qr
5
CHARGE PUMP
φr
φp
18
25
Qp
19
Gp
24
Tp
D Q
CL
12
17
21
D Q
p1
p2
D Q#
p3
CL
13
CL
14

FIG. 8

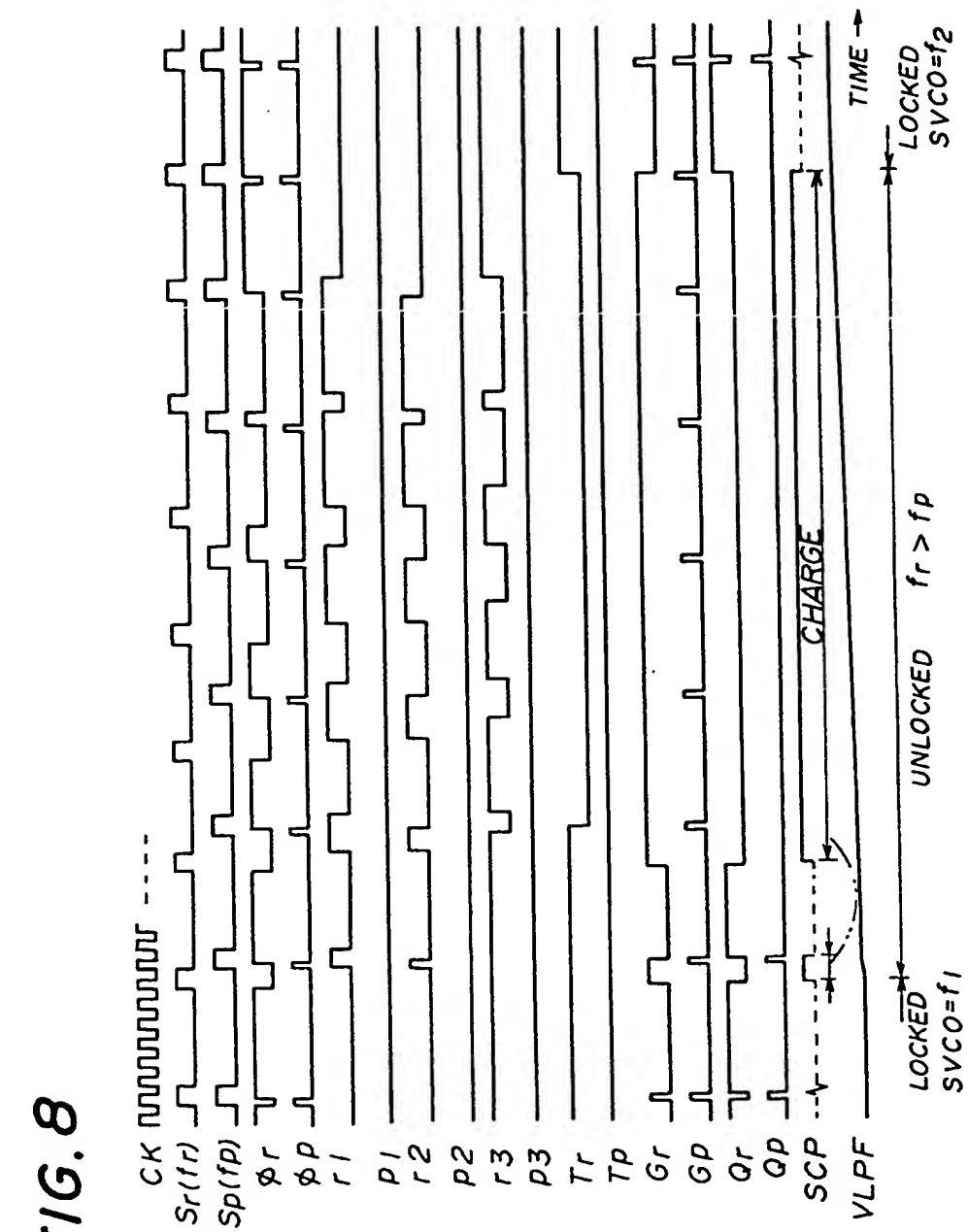

CK
Sr(fr)
Sp(fp)
φr
φp
r1
p1
r2
p2
r3
p3
Tr
Tp
Gr
Gp
Qr
Qp
SCP
VLPF
CHARGE
LOCKED
SVCO=f1
UNLOCKED
fr > fp
TIME
LOCKED
SVCO=f2

FIG.9

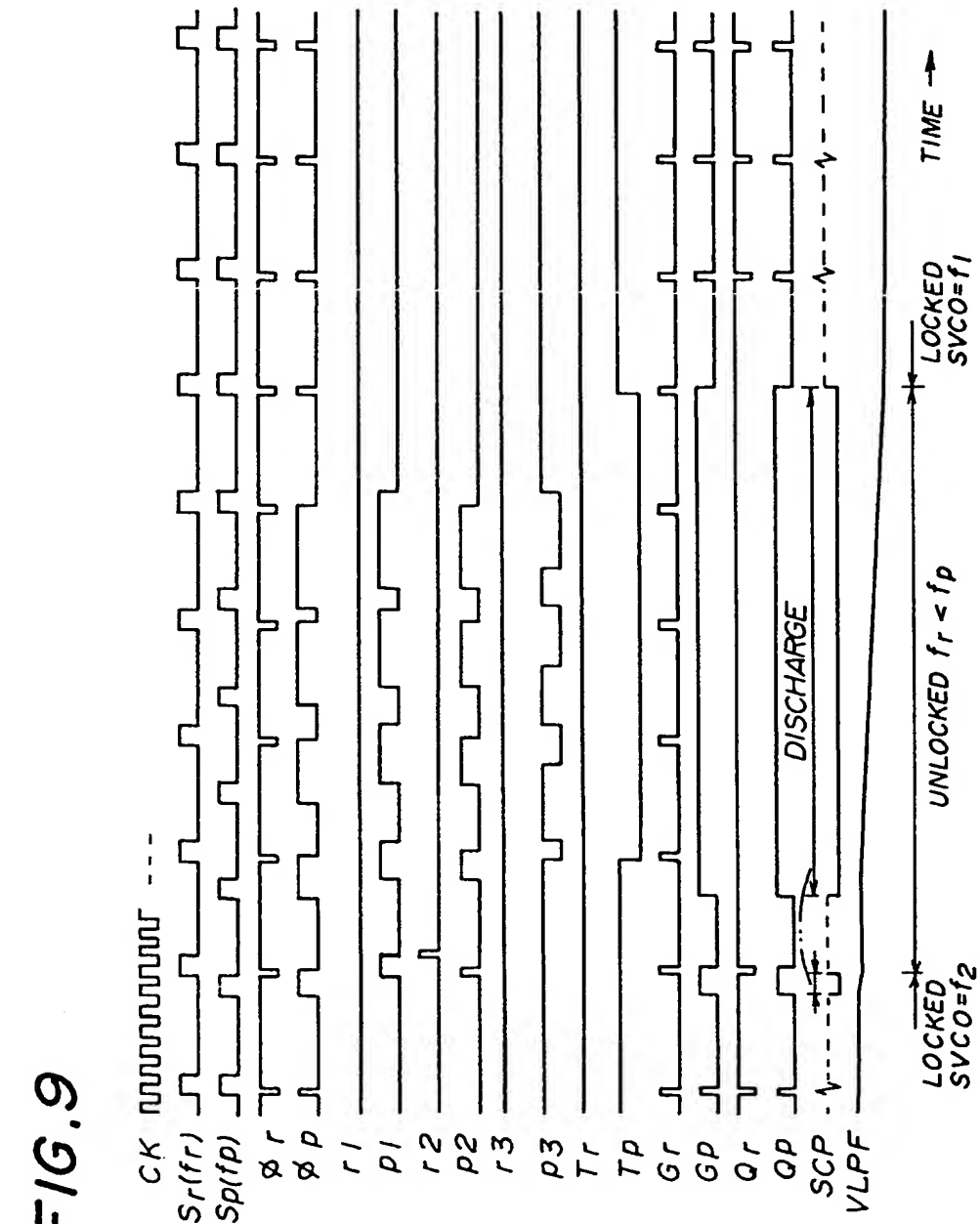

CK
Sr(fr)
Sp(fp)
ϕr
ϕp
r1
p1
r2
p2
r3
p3
Tr
Tp
Gr
Gp
Qr
Qp
SCP
VLPF
DISCHARGE
LOCKED SVCO=f2
UNLOCKED fr < fp
LOCKED SVCO=f1
TIME

FIG. 10

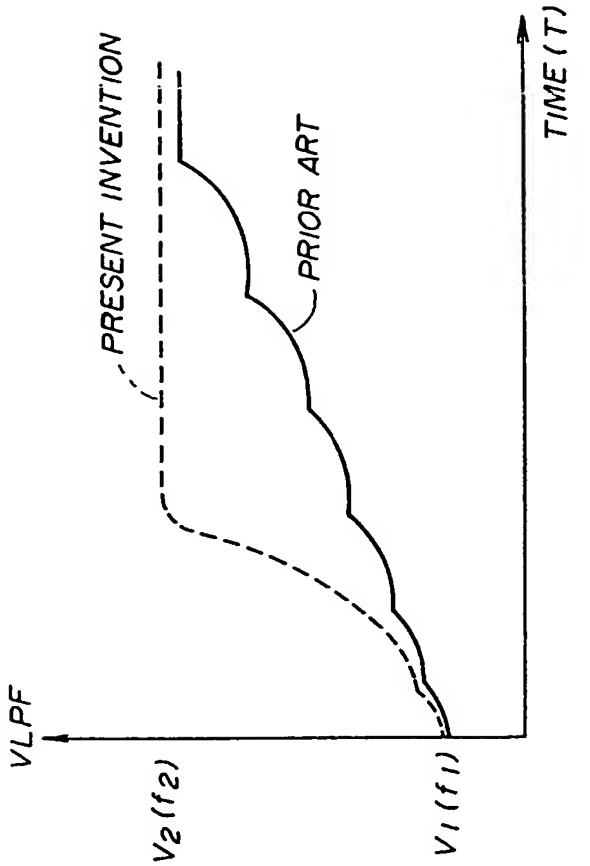
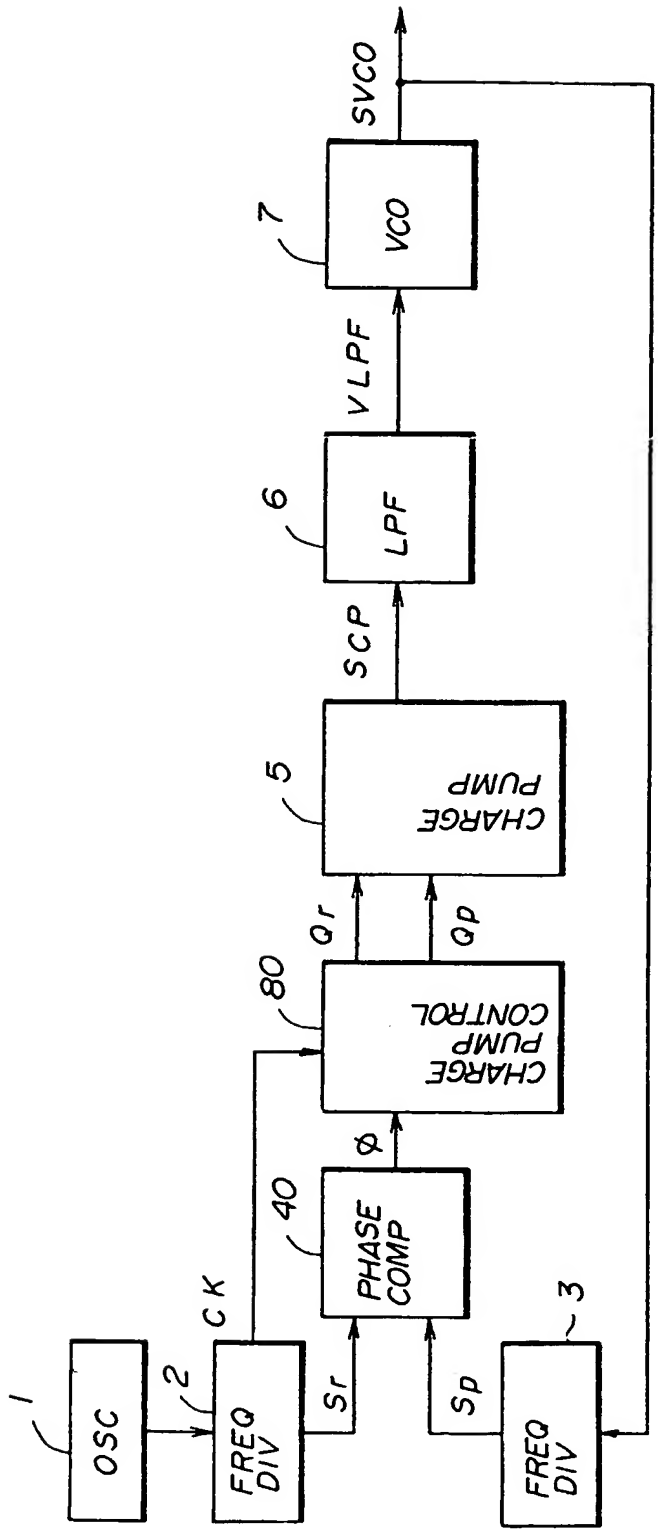


FIG.11


OSC
1
2
FREQ DIV
CK
Sr
PHASE COMP
40
φ
CHARGE PUMP CONTROL
80
Qr
Qp
CHARGE PUMP
5
SCP
LPF
6
VLPF
VCO
7
SVCO
Sp
FREQ DIV
3